**Course Objective:**  
To introduce basic principles of digital logic design, its implementation and applications.

1. **Introduction (3 hours)**
   1. Definitions for Digital Signals
   2. Digital Waveforms
   3. Digital Logic
   4. Moving and Storing Digital Information
   5. Digital Operations
   6. Digital Computer
   7. Digital Integrated Circuits
   8. Digital IC Signal Levels
   9. Clock wave form
   10. Coding
       1. ASCII Code
       2. BCD
       3. The Excess – 3 Code
       4. The Gray Code

1. **Digital Logic(1 hour)**
   1. The Basic Gates: NOT, OR, AND
   2. Universal Logic Gates: NOR, NAND
   3. AND-OR-INVERT Gates
   4. Positive and Negative Logic
   5. Introduction to HDL

1. **Combinational Logic Circuits(5 hours)**
   1. Boolean Laws and Theorems
   2. Sum-of-Products Method
   3. Truth Table to Karnaugh Map
   4. Pairs, Quads, and Octets
   5. Karnaugh Simplifications
   6. Don’t Care Conditions
   7. Product of Sums Method
   8. Product of Sums Simplification
   9. Hazards and Hazard Covers
   10. HDL Implementation Models

1. **Data Processing Circuits(5 hours)**
   1. Multiplexetures
   2. Demultiplexetures
   3. Decoder
   4. BCD-to-Decimal Decoders
   5. Seven-Segment Decoders
   6. Encoder
   7. Exclusive-OR Gates
   8. Parity Generators and Checkers
   9. Magnitude Comparator
   10. Read-Only Memory
   11. Programmable Array Logic
   12. Programmable Logic Arrays
   13. Troubleshooting with a Logic Problems
   14. HDL Implementation of Data Processing Circuits

1. **Arithmetic Circuits(5 hours)**
   1. Binary Addition
   2. Binary Subtraction
   3. Unsigned Binary Numbers
   4. Sign-Magnitude Numbers
   5. 2’s Complement Representation
   6. 2’s Complement Arithmetic
   7. Arithmetic Building Blocks
   8. The Adder-Subtracter
   9. Fast Adder
   10. Arithmetic Logic Unit
   11. Binary Multiplication and Division
   12. Arithmetic Circuits Using HDL

1. **Flip Flops(5 hours)**
   1. RS Flip-Flops
   2. Gated Flip-Flops
   3. Edge-Triggered RS Flip-Flops
   4. Egde Triggered D Flip-Flops
   5. Egde Triggered JK Flip-Flops
   6. Flip-Flop Timing
   7. JK Mater- Slave Flip-Flops
   8. Switch Contacts Bounds Circuits
   9. Various Representation of Flip-Flops
   10. Analysis of Sequencial Circuits

1. **Registers(2 hours)**
   1. Types of Registers
   2. Serial In–Serial Out
   3. Serial In–Parallel Out
   4. Parallel In–Serial Out
   5. Parallel In–Parallel Out
   6. Applications of Shift Registers

1. **Counters(5 hours)**
   1. Asynchronous Counters
   2. Decoding Gates
   3. Synchronous Counters
   4. Changing the Counter Modulus
   5. Decade Counters
   6. Presettable Counters
   7. Counter Design as a Synthesis Problem
   8. A Digital Clock

1. **Sequential Machines(8 hours)**
   1. Synchronous Machines
      1. Clock Driven Models and State Diagrams
      2. Transition tables, Redundant States
      3. Binary Assignment
      4. Use of Flip-Flops in realizing the models
   2. Asynchronous Machines
      1. Hazards in Asynchronous System and Use of Redundant Branch
      2. Allowable Transitions
      3. Flow tables and Merger Diagrams
      4. Excitation Maps and Realization of the models

1. **Digital Integrate Circuits(4 hours)**
   1. Switching Circuits
   2. 7400 TTL
   3. TTL parameters
   4. TTL Overvew
   5. Open Collecter Gates
   6. Three-state TTL Devices
   7. External Drive for TTL Lods
   8. TTL Driving External Loads
   9. 74C00 CMOS
   10. CMOS Characteristics
   11. TTL-to–CMOS Interface
   12. CMOS-to-TTL Interface

1. **Applications(2 hours)**
   1. Multiplexing Displays
   2. Frequency Counters
   3. Time Measurement

**Practical:**

1. DeMorgan’s law and it’s familiarization with NAND and NOR gates
2. Encoder, Decoder, and Multiplexer
3. Familiarization with Binary Addition and Subtraction
4. Construction of True Complement Generator
5. Latches, RS, Master-Slave and T type flip flops
6. D and JK type flip flops
7. Ripple Counter, Synchronous counter
8. Familiarization with computer package for logic circuit design
9. Design digital circuits using hardware and software tools
10. Use of PLAs and PLDs

**References:**

1. Donald P. Leach, Albert Paul Malvino and  Goutam Saha, “ Digital Principles and Applications”, 6th edition , Tata McGraw-Hill, 2006
2. David  J Comer “Digital Logic And State Machine Design” 3rd edition, Oxfored University Press, 2002
3. William I. Fletcher “An Engineering Approach  to Digital Design” Printice Hall of India, New Delhi 1990
4. William H. Gothmann, “Digital Electronics, An Introduction to Theory and Practice”, 2nd edition, PHI, 2009

**Evaluation Scheme:**  
The questions will cover all the chapters of the syllabus. The evaluation scheme will be as indicated in the table below

|  |  |  |
| --- | --- | --- |
| **Chapters** | **Hours** | **Marks distribution\*** |
| 1 | 3 | 6 |
| 2 | 1 | 4 |
| 3 | 5 | 8 |
| 4 | 5 | 10 |
| 5 | 5 | 8 |
| 6 | 5 | 8 |
| 7 | 2 | 4 |
| 8 | 5 | 8 |
| 9 | 8 | 12 |
| 10 | 4 | 8 |
| 11 | 2 | 4 |
| Total | 45 | 80 |

**\*Note: There may be a minor deviation in the marks distribution.**